Page 11, line 35 - page 12, line 11, delete current paragraph and insert therefor:

a2 In this embodiment, a third insulating layer 13 is formed on the light shielding layer 12, and a rectangular pixel electrode 14 as a reflective electrode almost corresponding to one pixel is formed on the third insulating layer 13 as shown in Figure 3. A contact hole 16 is provided inside the opening 12a in the light shielding film 12 so as to pierce the third insulating interlayer 13 and the second insulating interlayer 11, and the contact hole 16 is filled with a pillar connecting plug 15 composed of a high melting point metal, such as tungsten, which electrically connects the auxiliary bonding wire 10 and the pixel electrode 14. A passivation film 17 is formed on the entire pixel electrode 14.

Page 30, line 10 - page 31, line 2, delete current paragraph and insert therefor:

a3 Figure 17 is a cross-sectional view of a configuration of a pixel in a reflective liquid crystal panel substrate. Figure 17 is a cross-sectional view along line I-I in the planar layout in Figure 3, as in Figure 1. In this embodiment, a TFT is used as a transistor for switching pixels. In Figure 17, the sections having the same identification numbers as Figures 1 and 2 represent the layers and the semiconductor regions having the same functions as in those drawings. Identification number 1 represents a quartz or non-alkaline glass substrate, single-crystal, polycrystalline or amorphous silicon film, regions 5a, 5b, 5c and 8 are formed on the insulating substrate, and insulating films 4b and 9b having a double layer structure composed of a silicon oxide film formed by thermal oxidation and a silicon nitride film formed thereon by a CVD process are formed on the silicon film. An N-type impurity is doped in the regions 5a, 5b and 8 of the silicon film before the formation of the upper silicon nitride film among the insulating film 4b to form a source region 5a and a drain region 5b of the TFT and an electrode region 8 of the holding capacitor. A wiring layer composed of polysilicon or a metal silicide is formed as a gate electrode 4a of the TFT and the other electrode 9a of the holding capacitor is formed on